USN | | | | | | | | | | |

06EC63

Sixth Semester B.E. Degree Examination, June/July 2014
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the characteristics and typical errors associated with sample and hold circuit. **(10 Marks)**

b. With reference to DAC describe. i) Resolution; ii) LSB; iii) DNL; iv) V_{FS}; v) Dynamic range; vi) INL. Find the value of 1LSB and V_{FS} for a 4-bit, 8-bit DAC V_{ref} = 5V. **(10 Marks)**

2 a. State the reasons for the pedestal error, droop aperture error and sampling error. **(08 Marks)**

b. Design a 4-bit charge scaling DAC using a split array. Assume that V_{ref} = 5V and that C = 0.5pF. Draw the equivalent circuit for D = 0001 and 0010 and determine the value of the output voltage. **(06 Marks)**

c. Discuss the issues involved in a mixed signal circuit layout. **(06 Marks)**

3 a. Explain the working principle and architecture of two step flash ADC. **(08 Marks)**

b. Assume that the two step ADC has four bits of resolution. Make a table listing the MSBs, V_1, V_2, V_3 and the LSBs, for V_{in} = 2, 4, 9 and 15V assuming that V_{ref} = 16V. **(04 Marks)**

c. For a 8 bit pipelined ADC, all the amplifiers had a gain of 2.1 J/V, instead of 2 V/V, If V_{in} = 3V and V_{ref} = 5V. What would be the resulting digital output, assuming other components ideal? **(08 Marks)**

4 a. Explain the purpose of each stage of a voltage comparator. Also explain the working of 1st stage in basic comparator design. **(10 Marks)**

b. Show that multiplying quad acts as a multiplier when all MOSFET's in the multiplying quad have the same threshold voltage. **(10 Marks)**

PART – B

5 a. Briefly explain the role of decimating filters in ADC. **(06 Marks)**

b. Discuss the advantages and disadvantages of cascading averaging circuits to increase filter attenuation. **(04 Marks)**

c. Describe with neat diagram, the conceptual layout and architectural layout of an R-2R resistor string with minimum area and also discuss the problems of laying out metal over the resistive material. **(10 Marks)**

6 a. Describe CMOS process flow with neat sketches. **(10 Marks)**

b. With the help of a block diagram, explain the accumulate and dump circuit. Plot the general frequency response of an averaging filter. **(10 Marks)**

7 a. Explain how capacitor and resistor elements are fabricated in submicron technology. **(07 Marks)**

b. Sketch the implementation of a synchronous up-down counter and discuss its operation. **(07 Marks)**

c. Explain the working of simple delay element using pass transistor and CMOS inverter. **(06 Marks)**

8 a. Illustrate how a pushpull output stage is biased with a floating current source. **(07 Marks)**

b. Explain the limitation of an inverter at the output of an op-amp with the help of its transfer curve. How is it overcome? **(07 Marks)**

c. Determine time constant of OPAMP with unity gain frequency of 100MHz. Assume that all the outputs is fed back to the input. Also determine the settling time for 0.1% settling accuracy. **(06 Marks)**

* * * * *